

FIG. 1

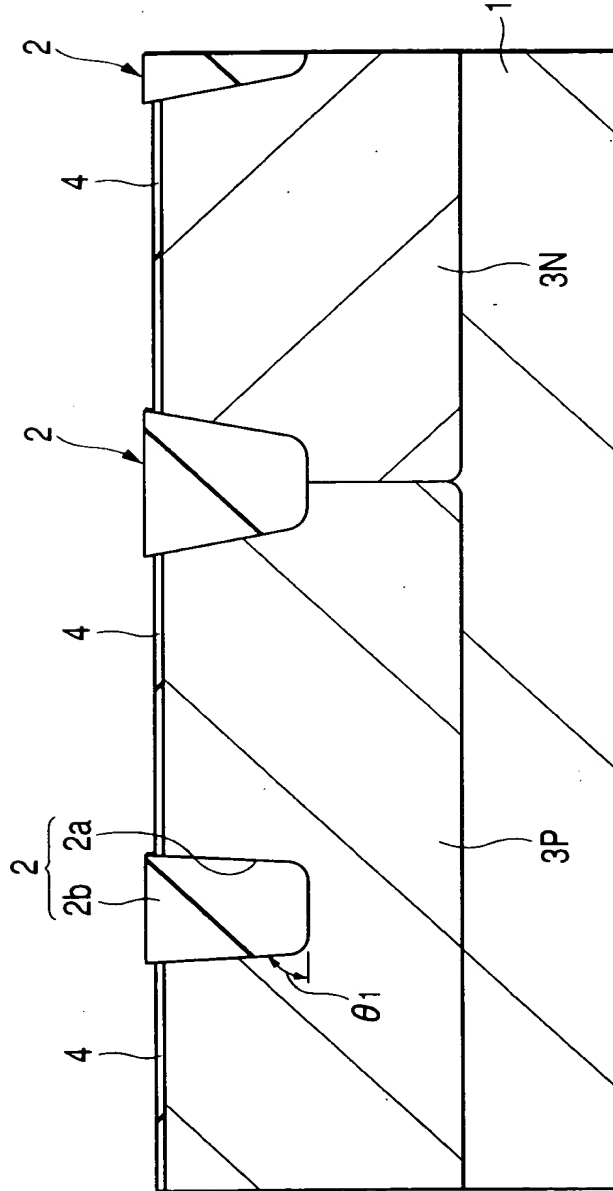


FIG. 2

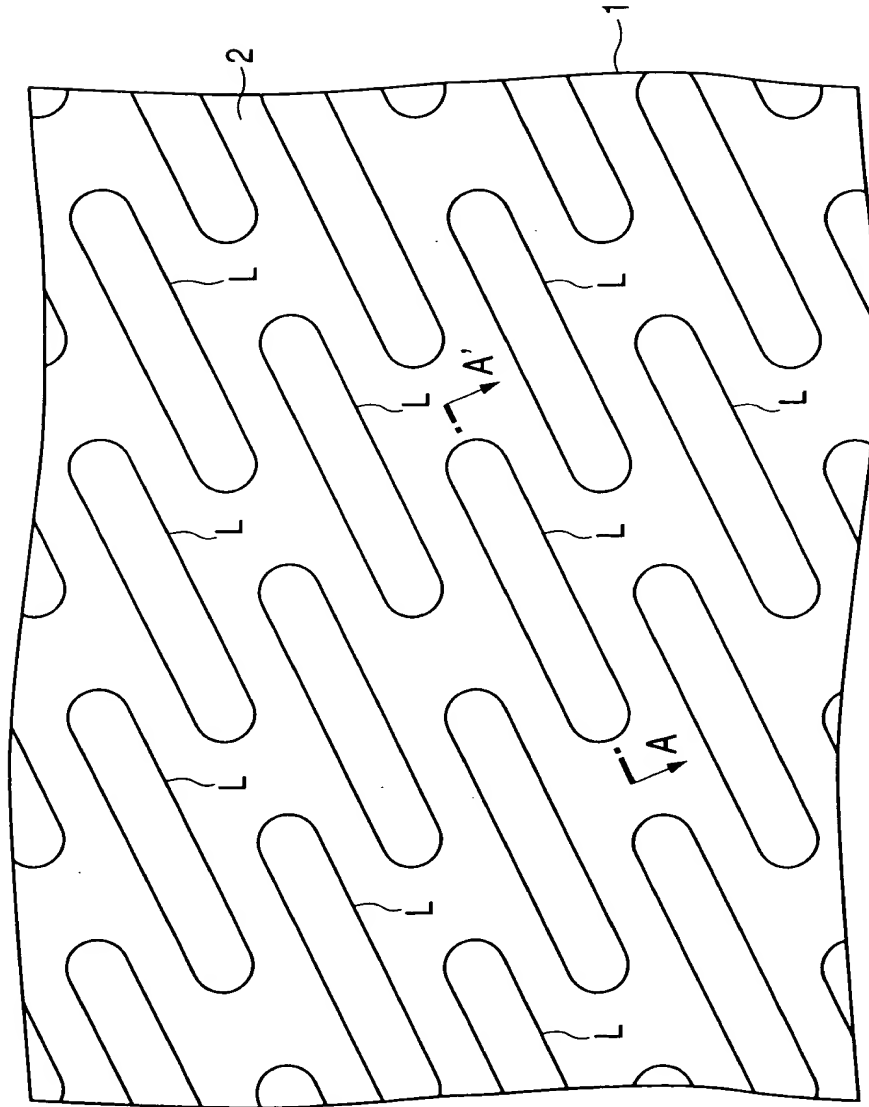


FIG. 3

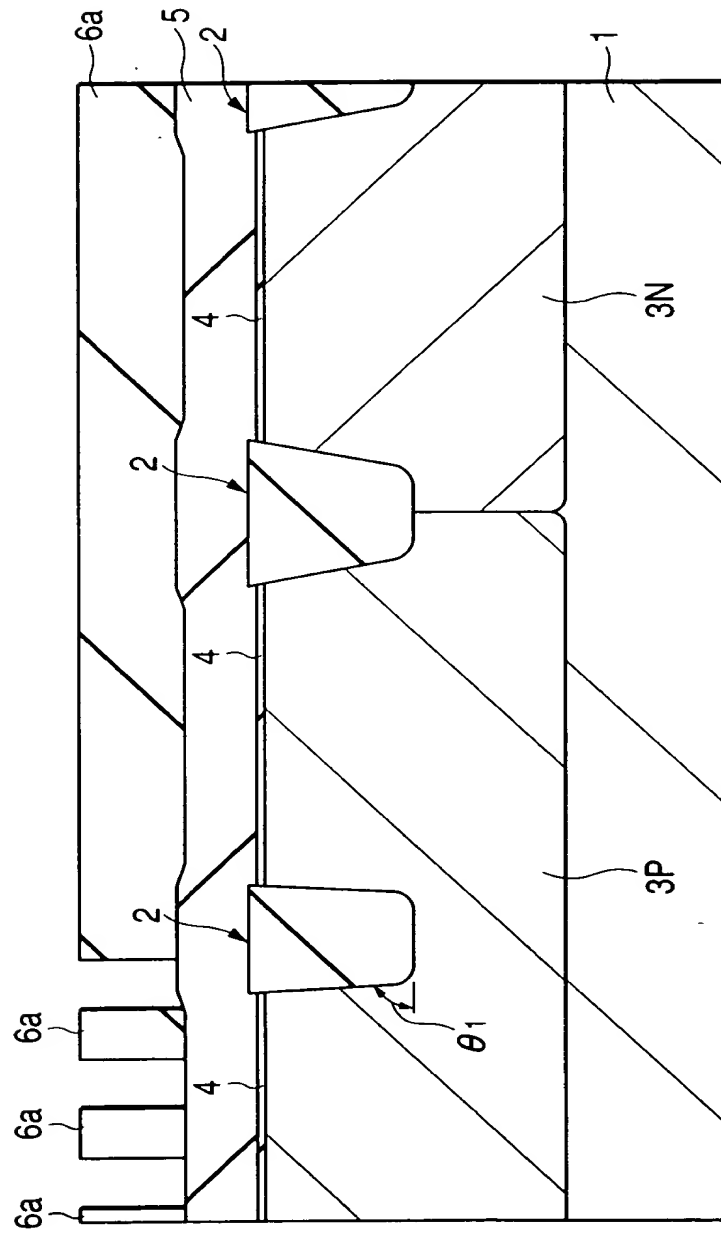


FIG. 4

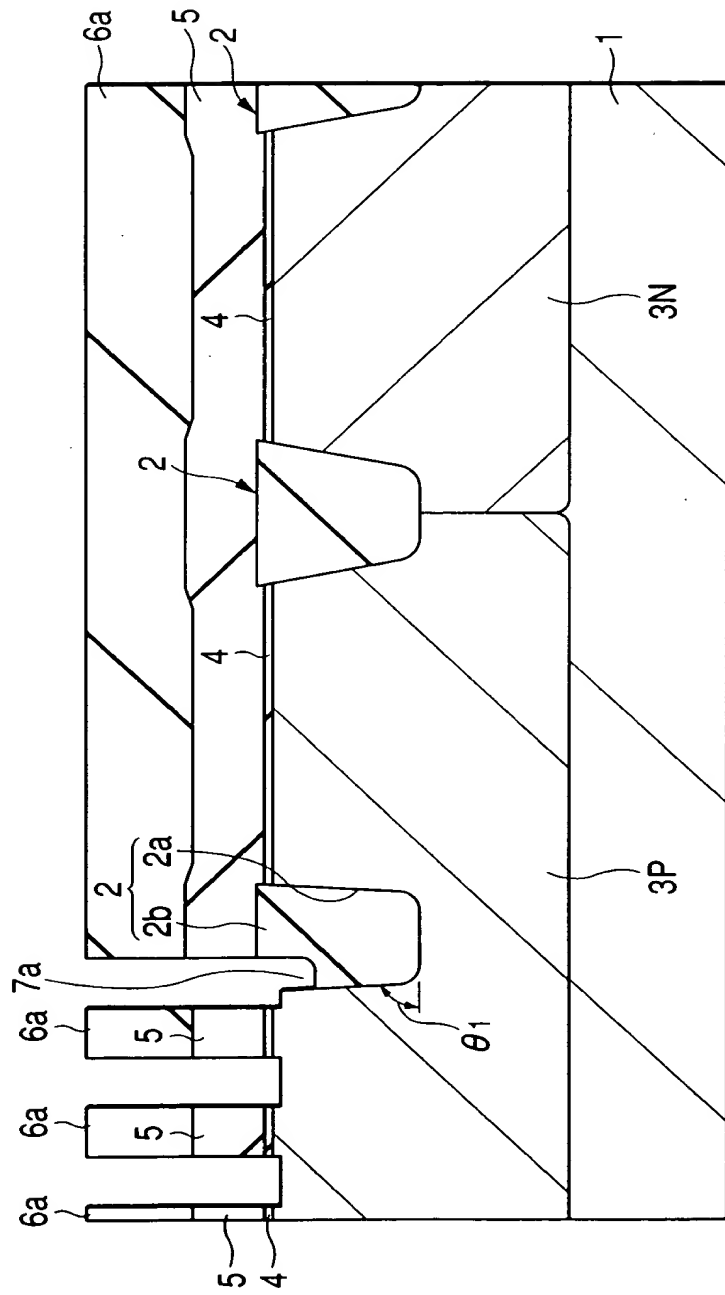


FIG. 6

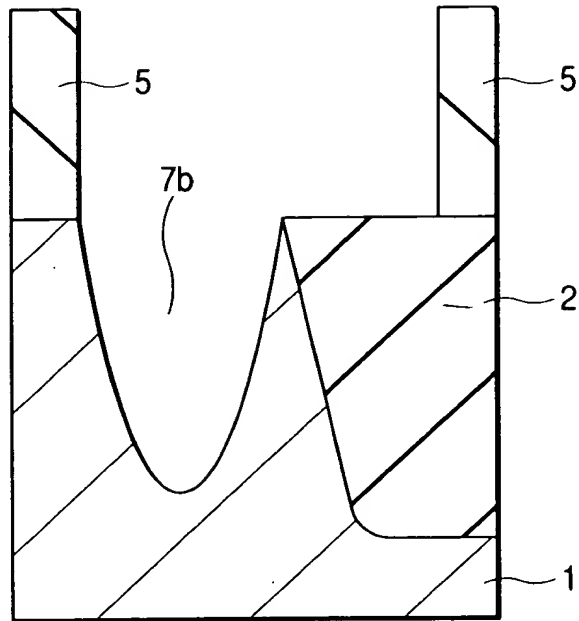


FIG. 7

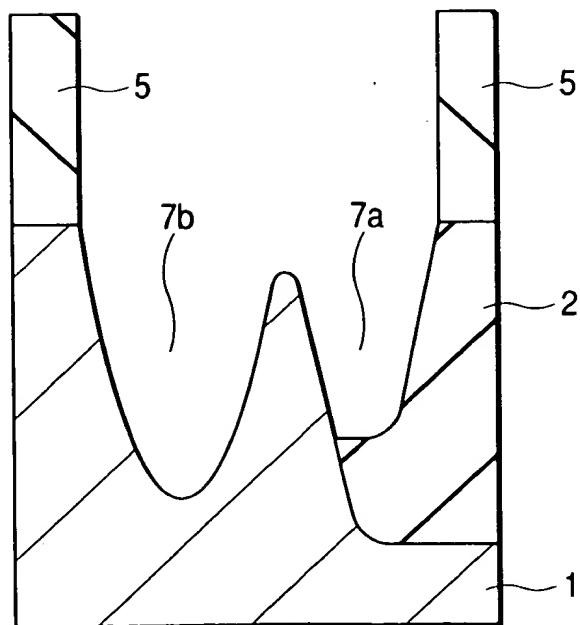


FIG. 8

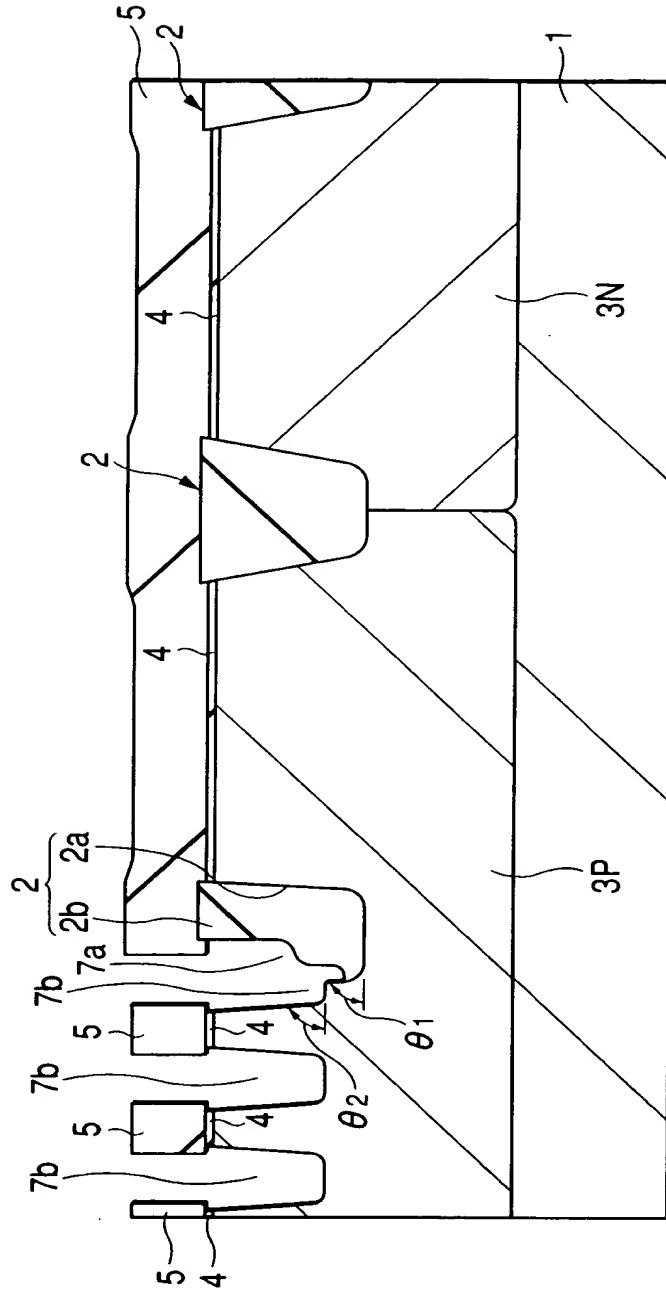


FIG. 10

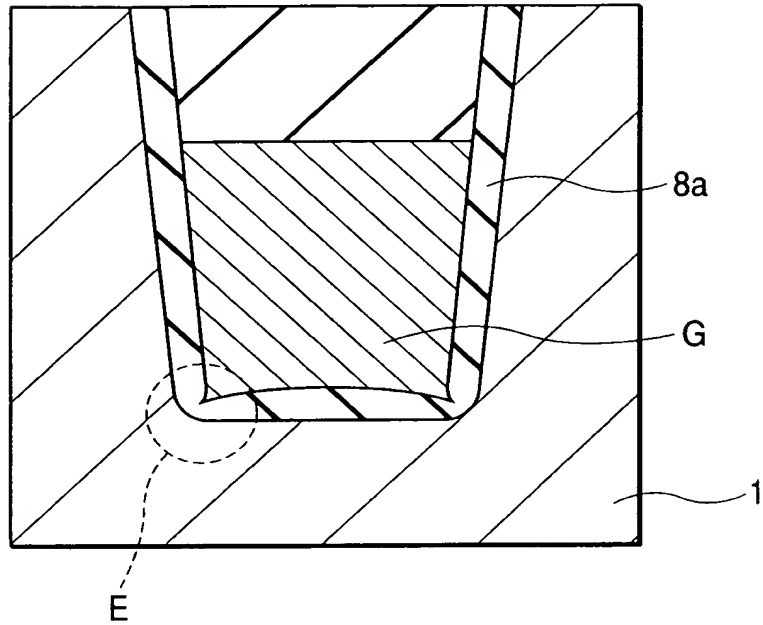


FIG. 11(a)

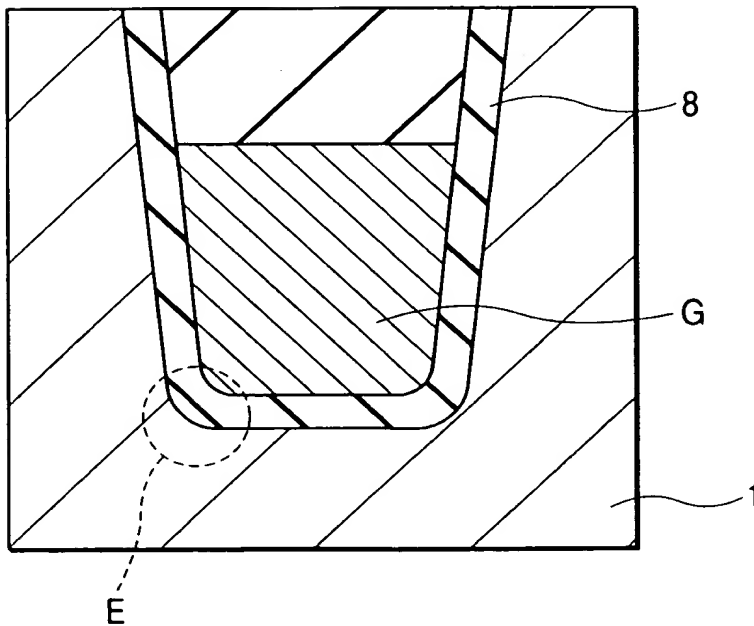


FIG. 11(b)

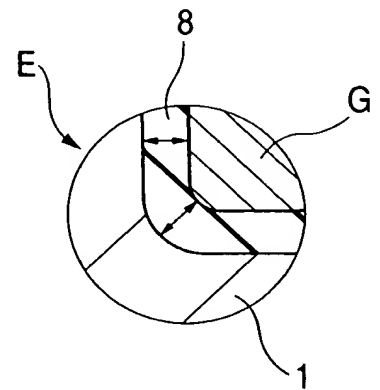


FIG. 12

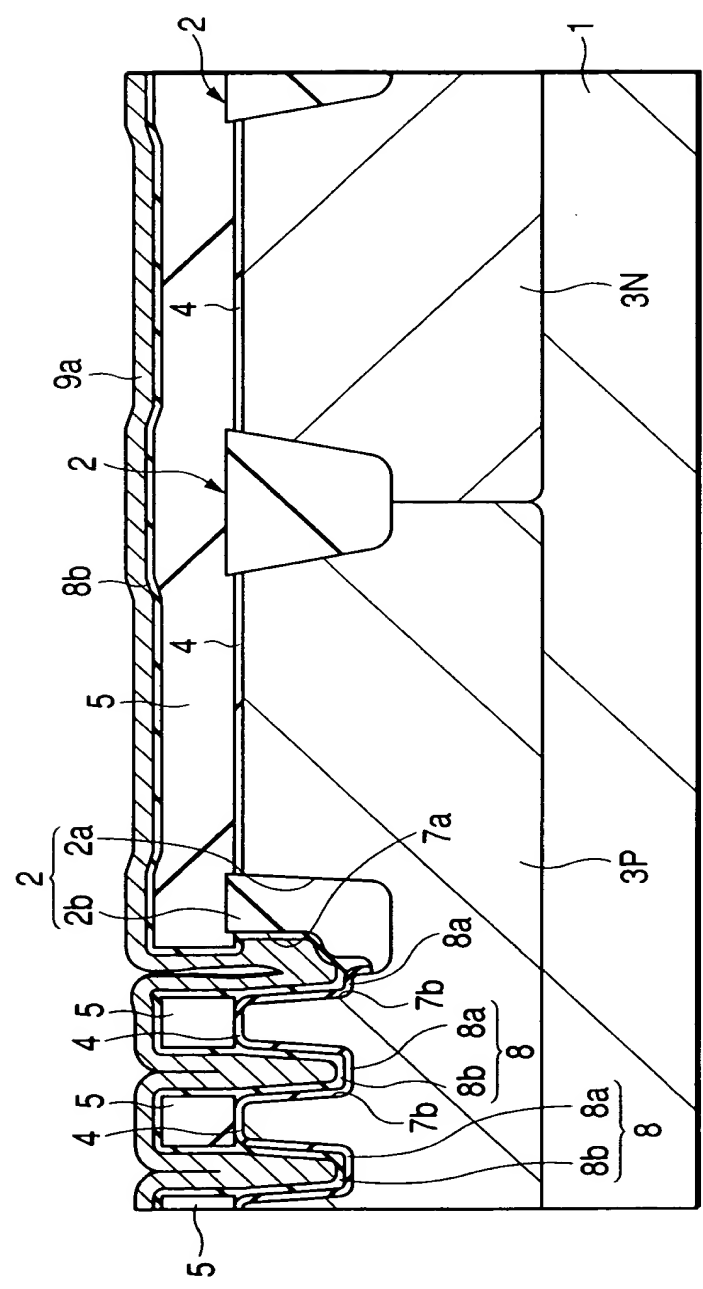


FIG. 13

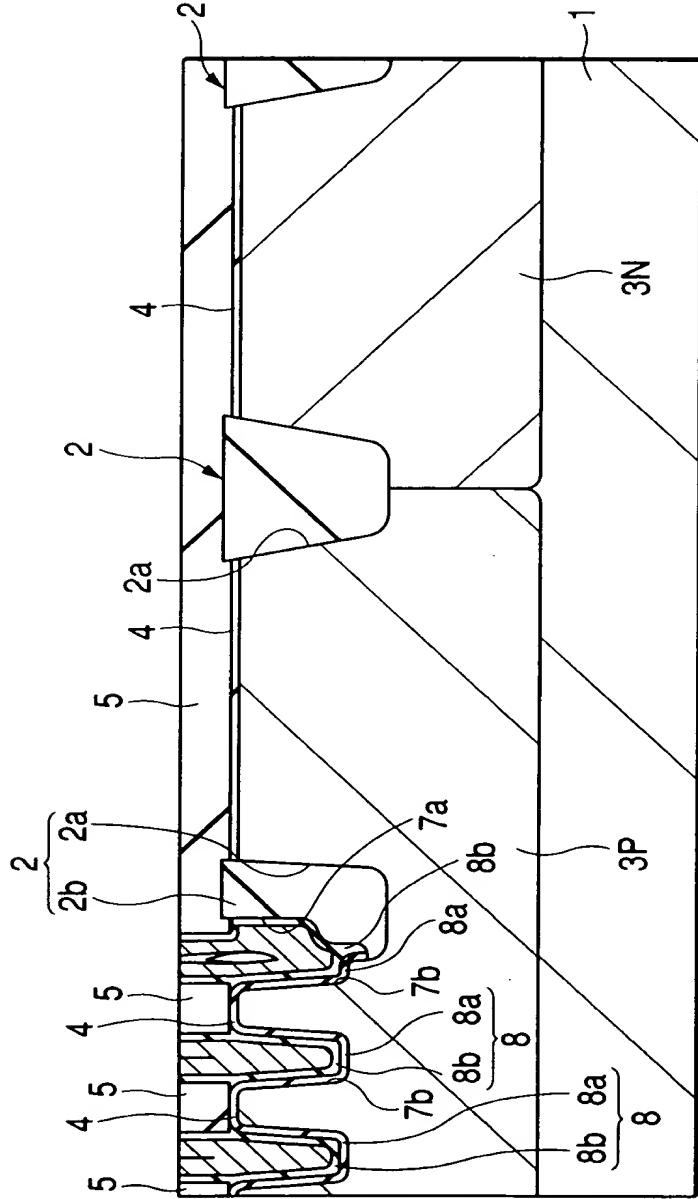


FIG. 15

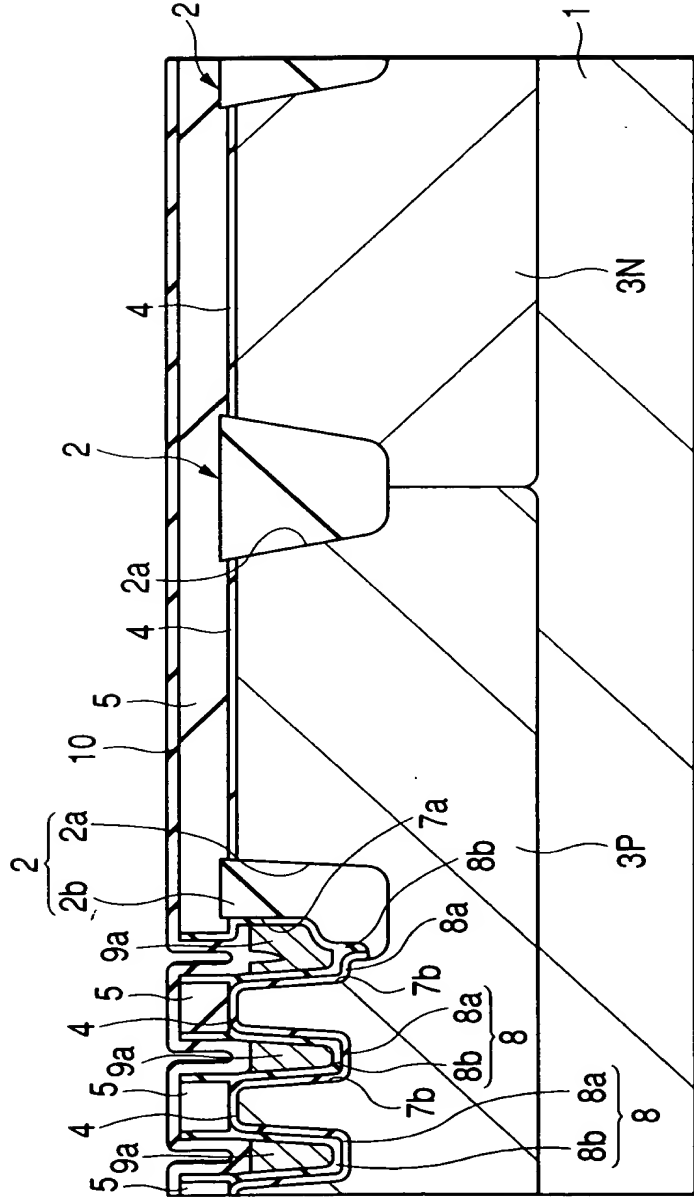


FIG. 17

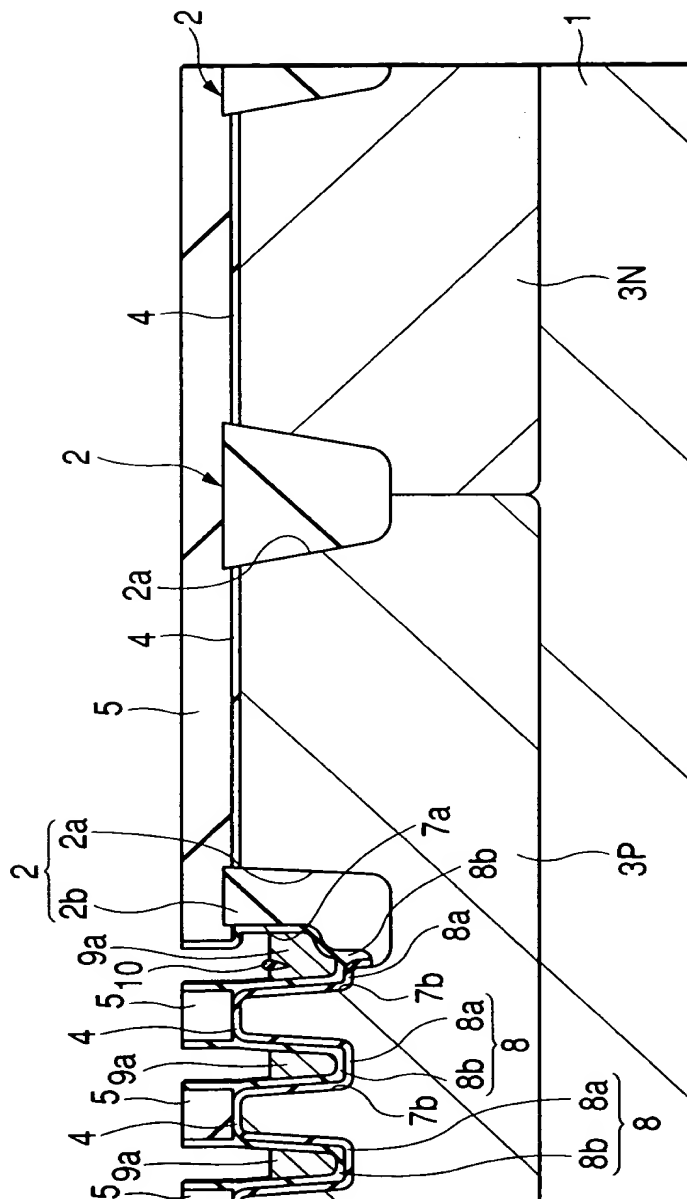


FIG. 18

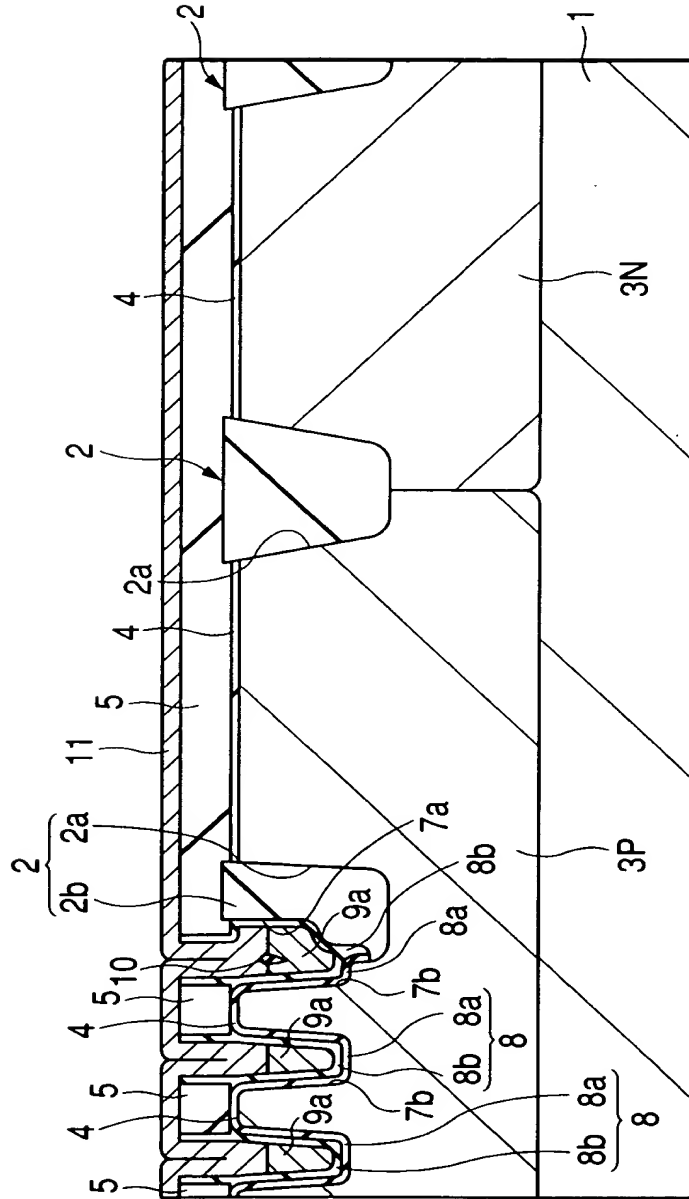


FIG. 19

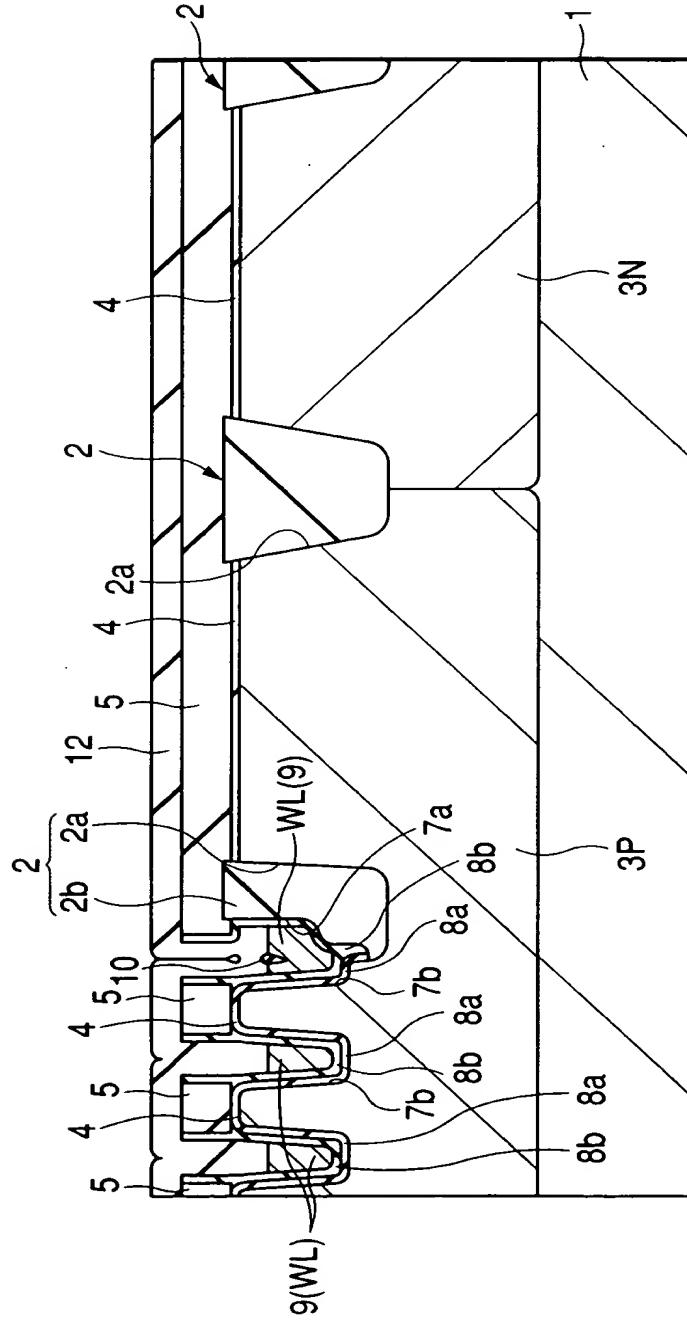


FIG. 20

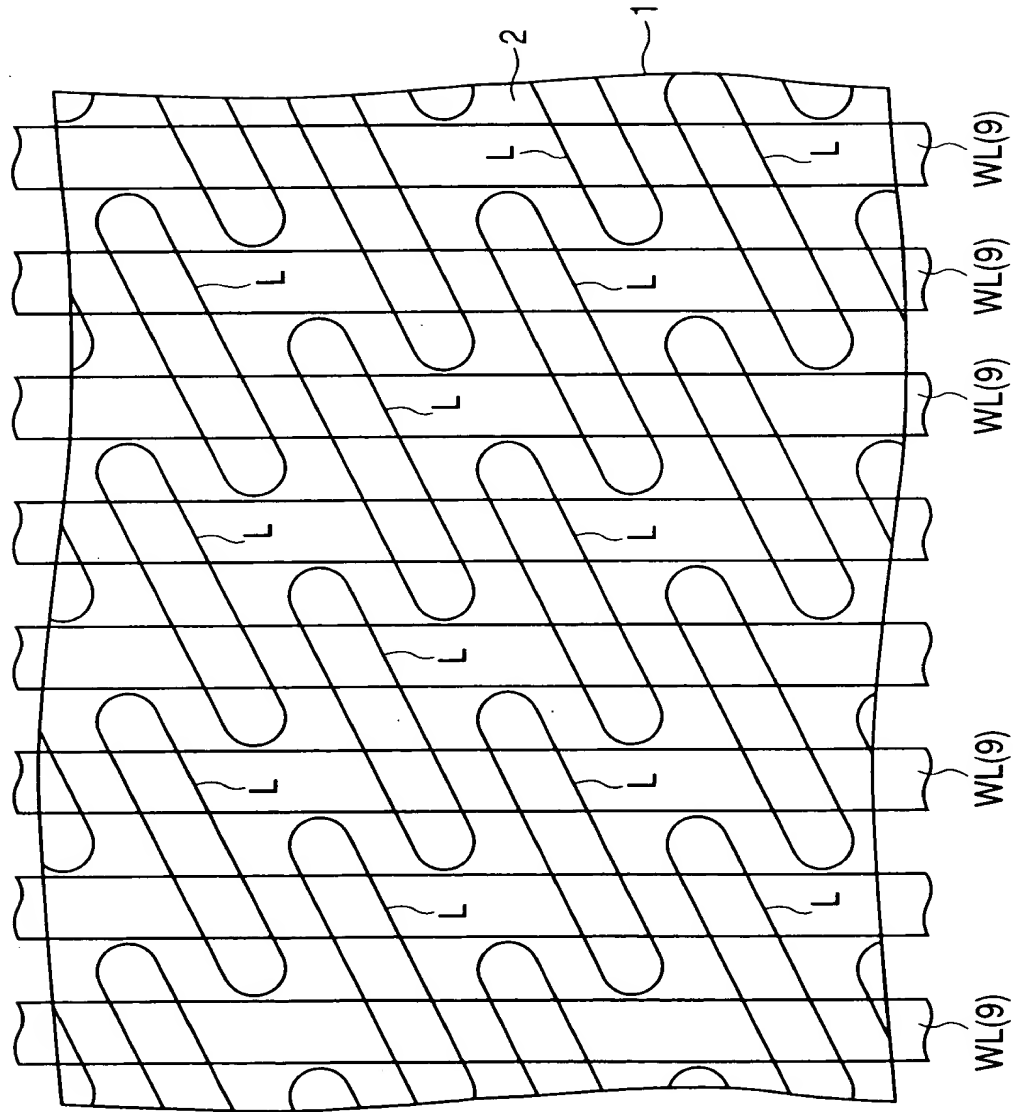
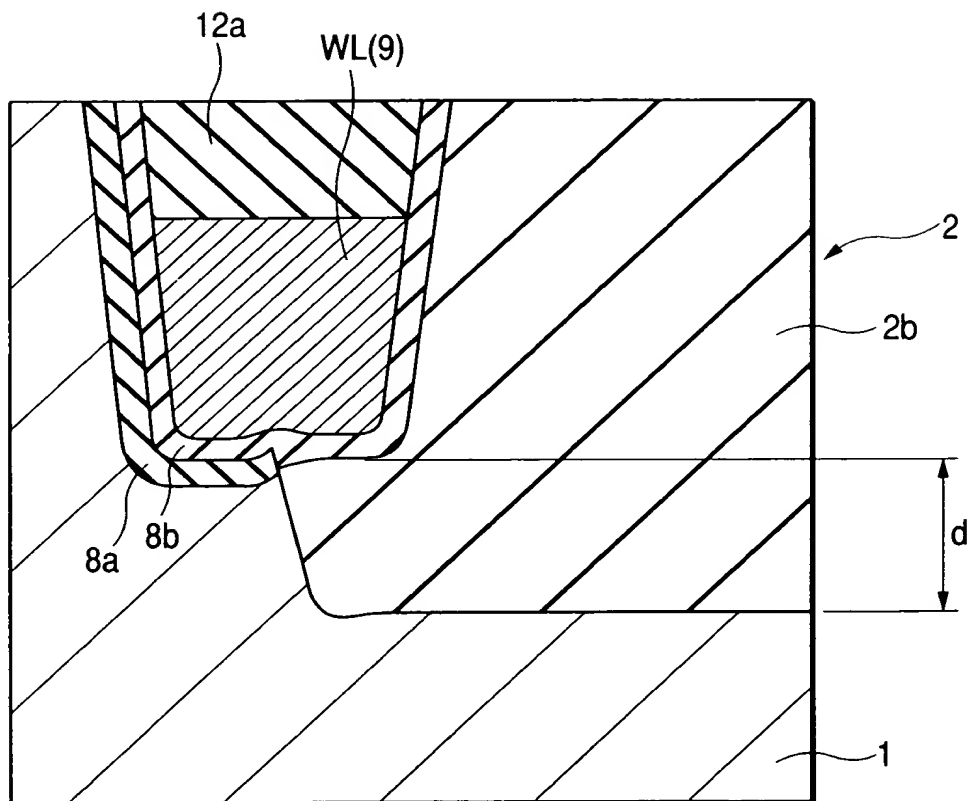


FIG. 22



This cross-sectional view illustrates the device structure. A gate stack (10) is formed on a substrate (1). The gate stack includes a gate dielectric (12) and a gate electrode (14). The gate electrode is connected to a gate line (9(WL)). Source/drain regions (15a, 15b) are formed in the substrate, and a source/drain electrode (16) is formed on top of them. A passivation layer (18) is formed over the device, and a contact pad (19) is formed in the passivation layer. The contact pad is connected to a contact line (20). The device is divided into three regions: 3P (passivation), 3N (nitride), and 3Q (quartz).

FIG. 26

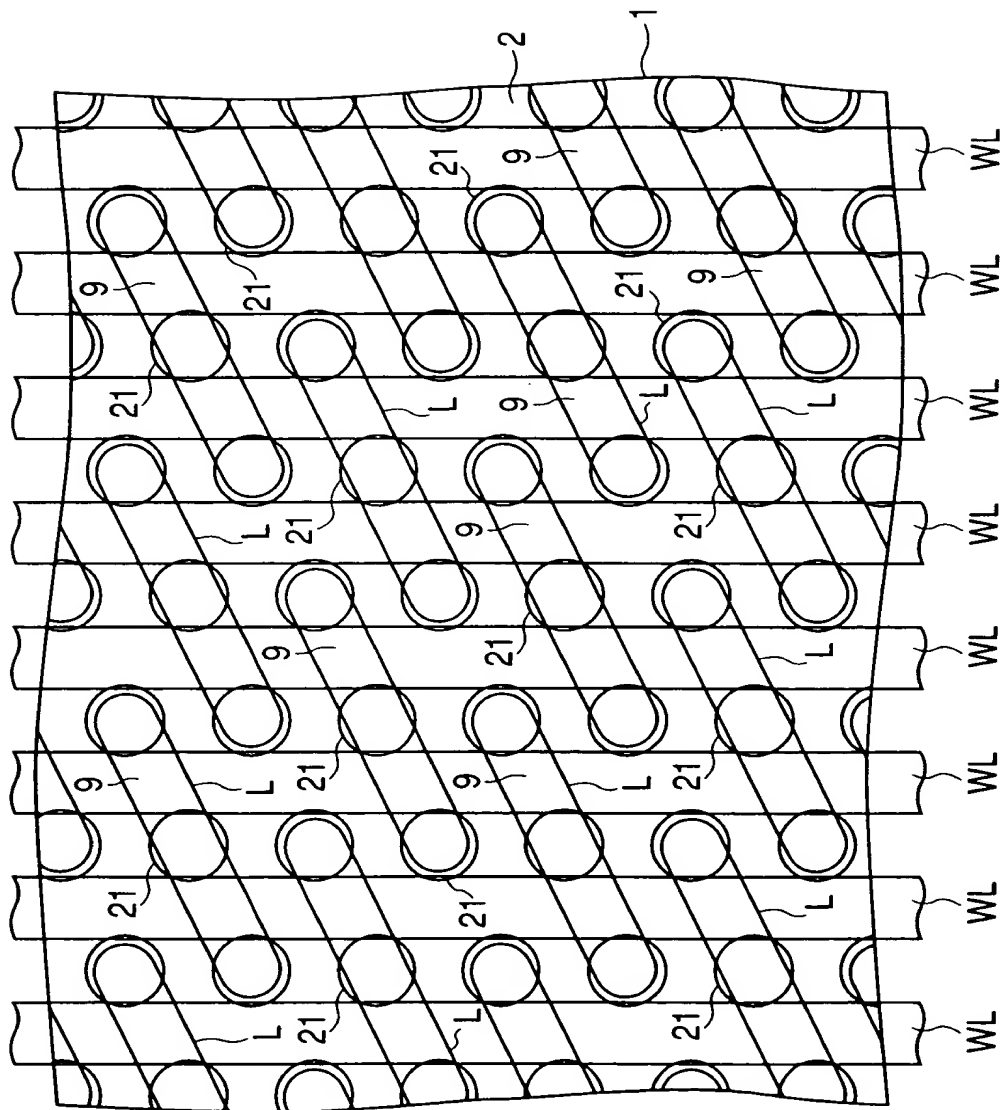


FIG. 27

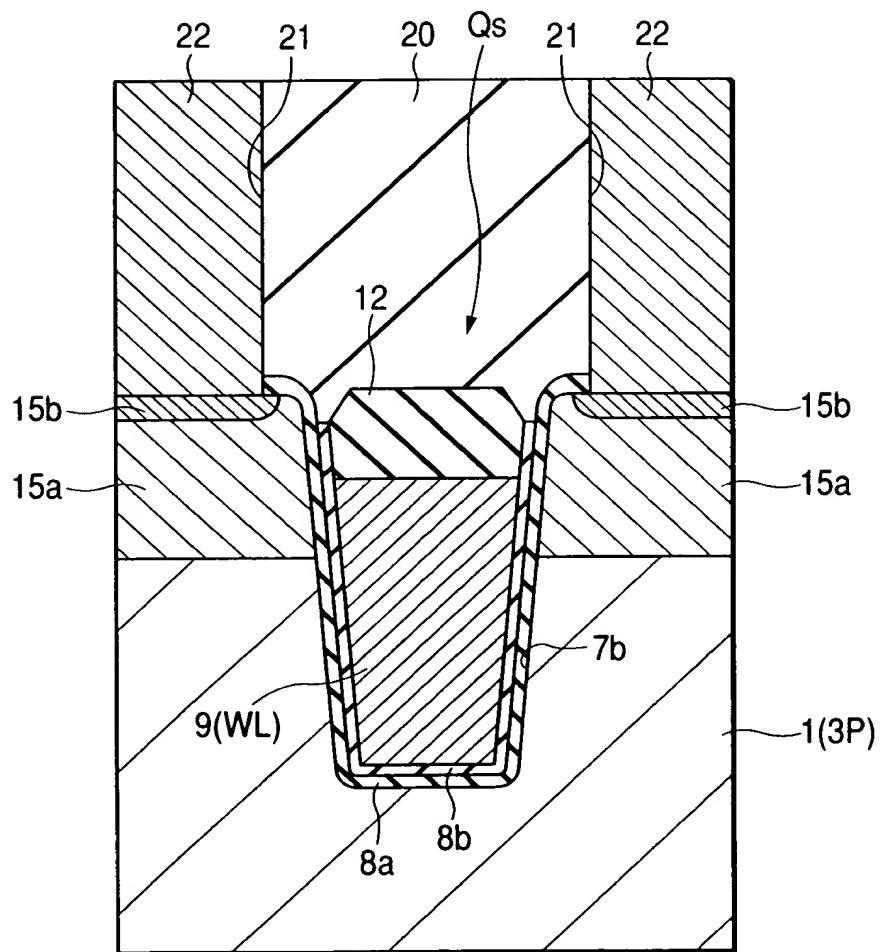


FIG. 28

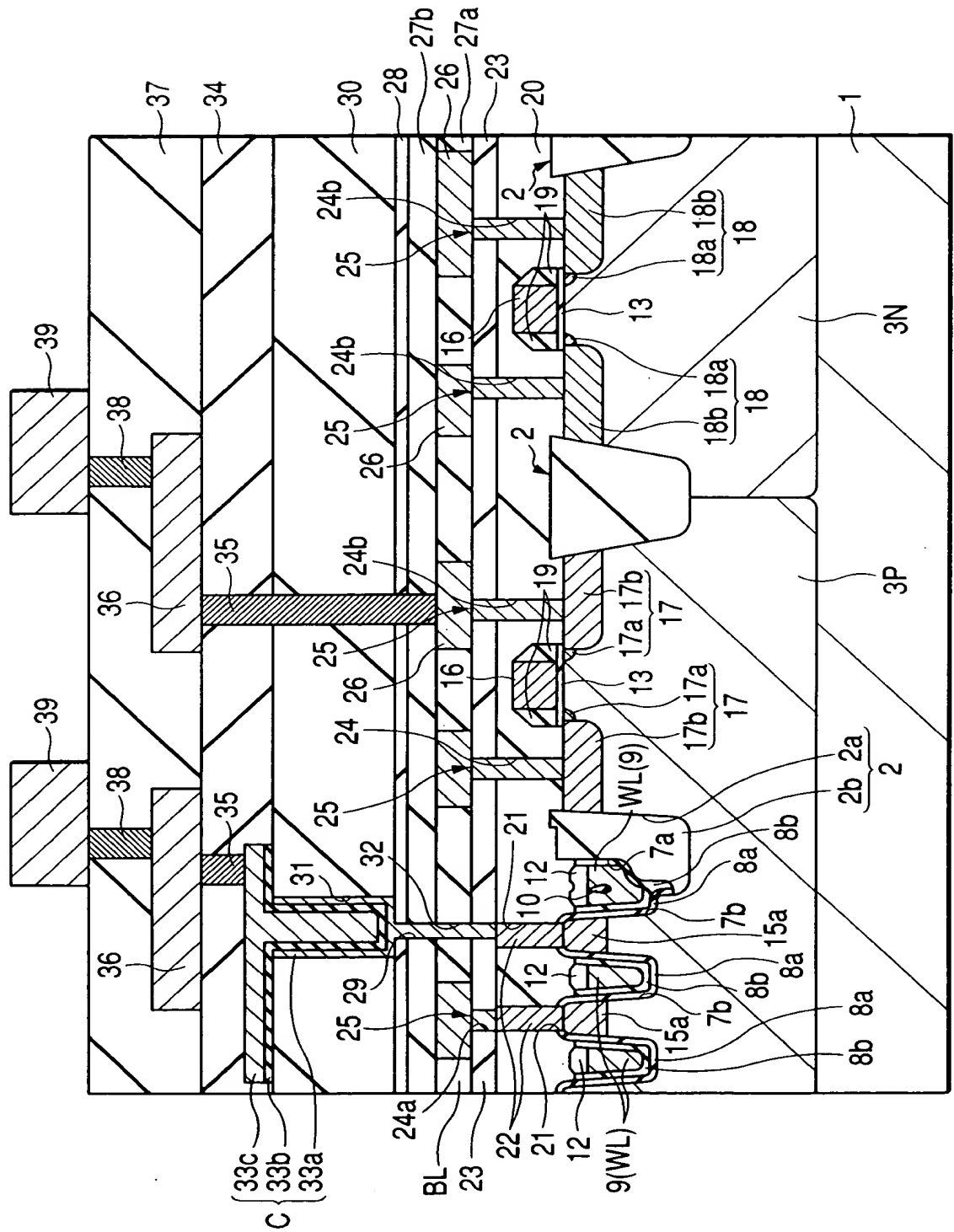


FIG. 29

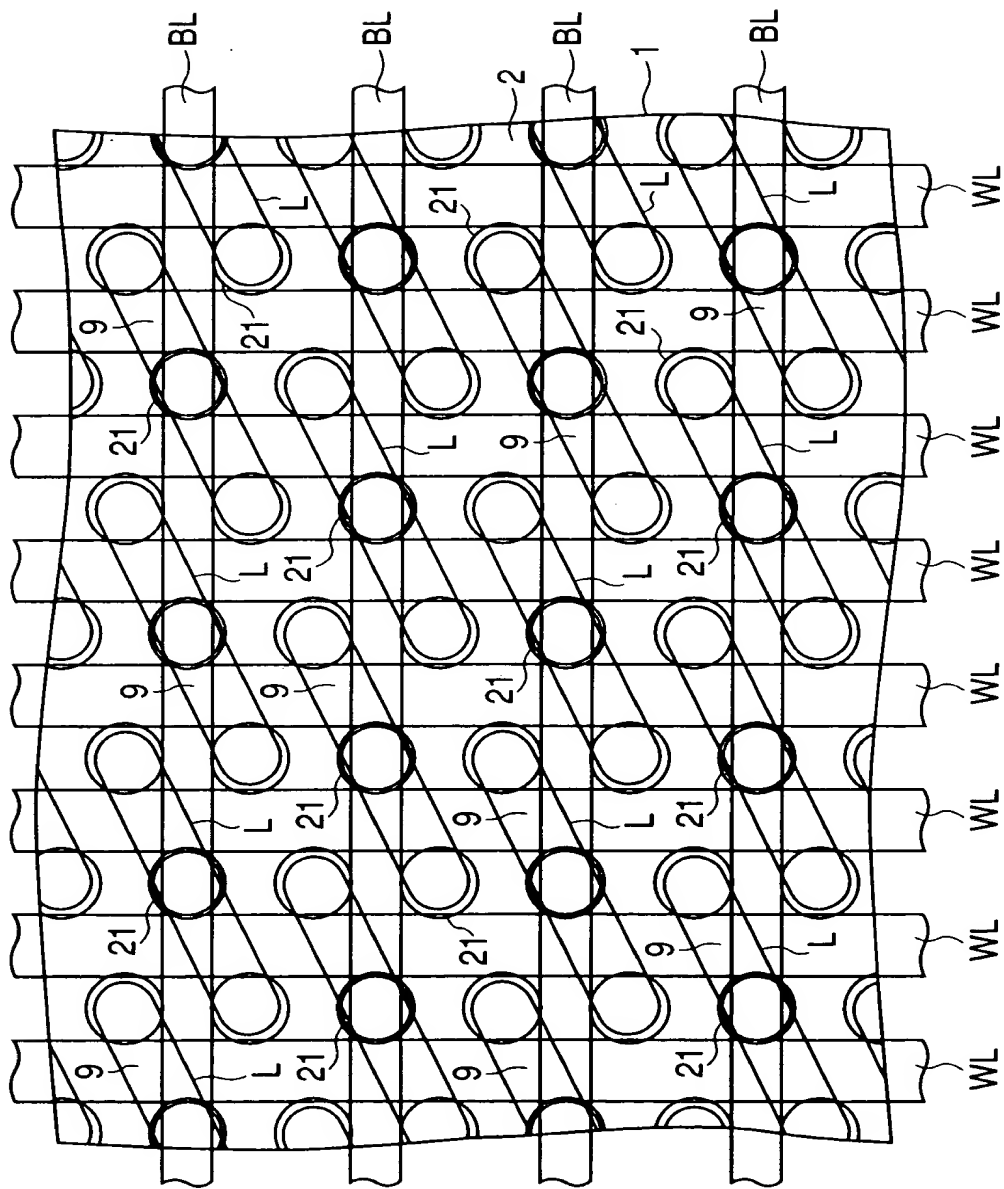


FIG. 30

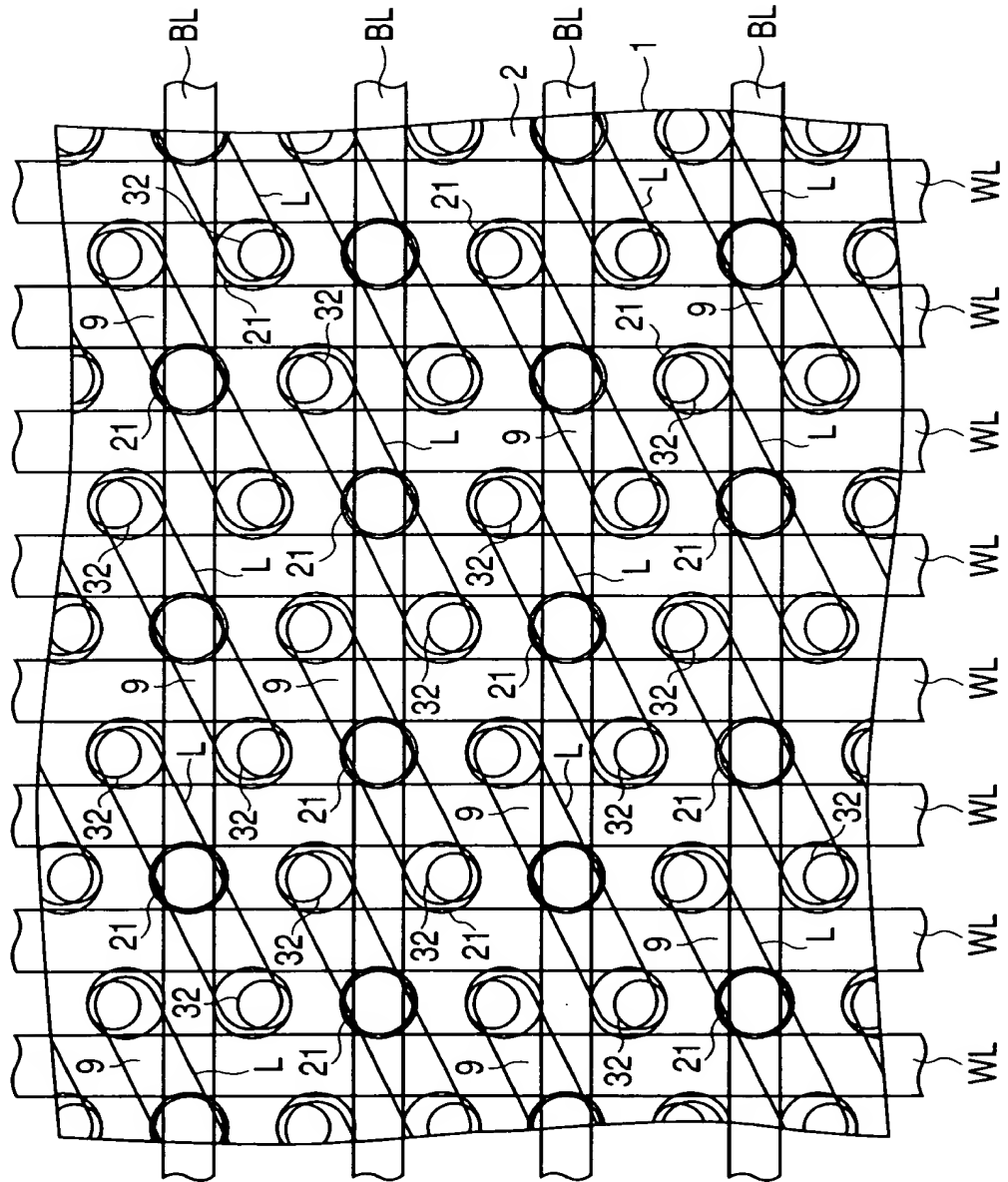


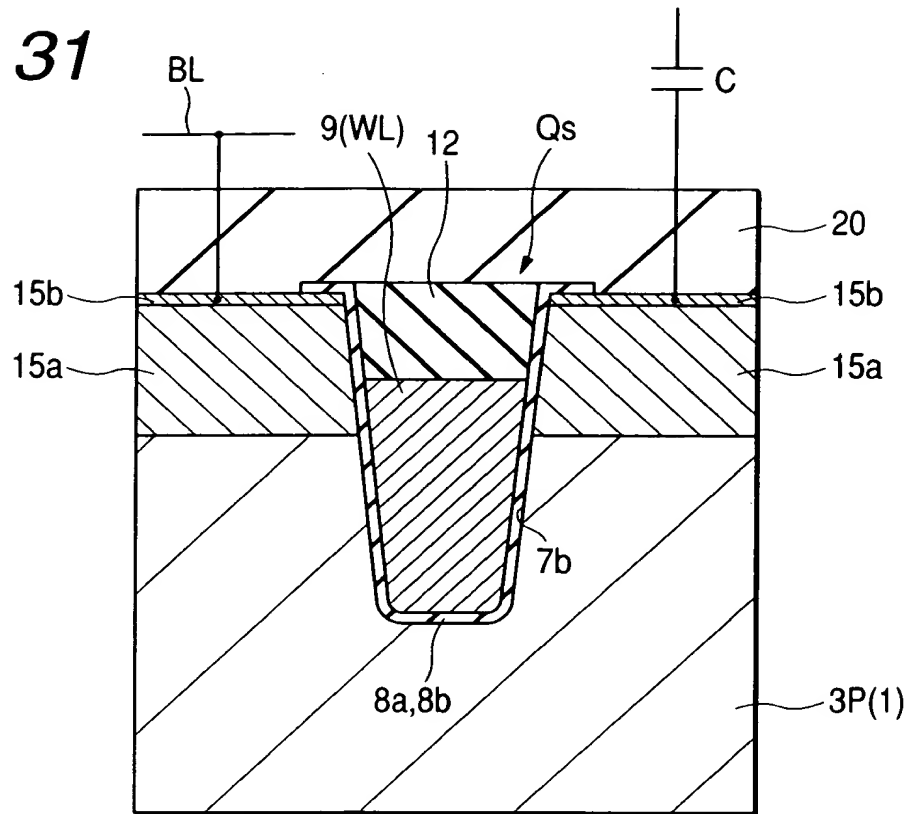
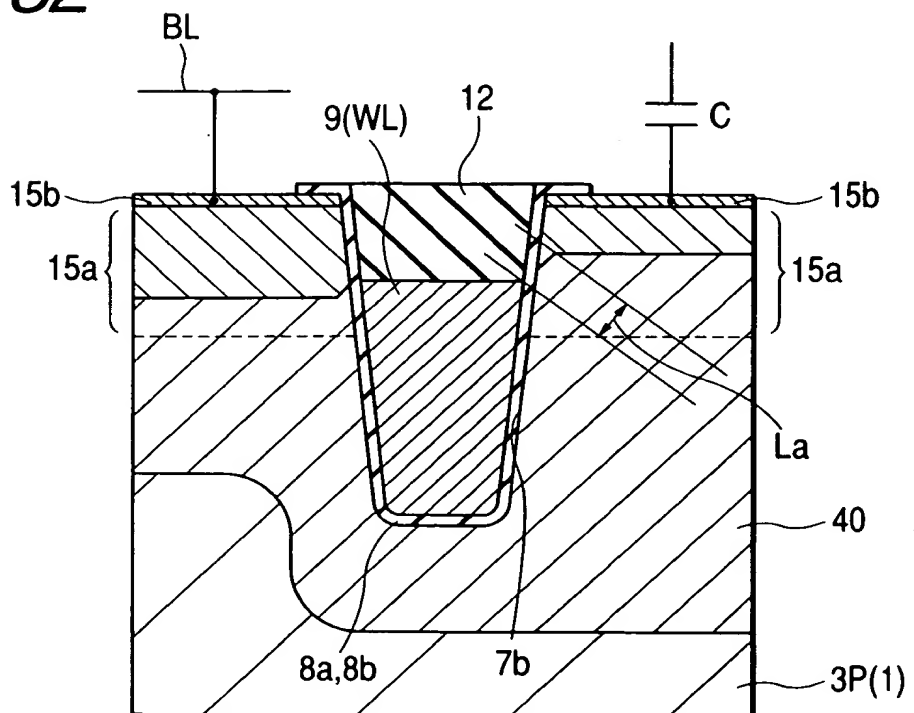
FIG. 31**FIG. 32**

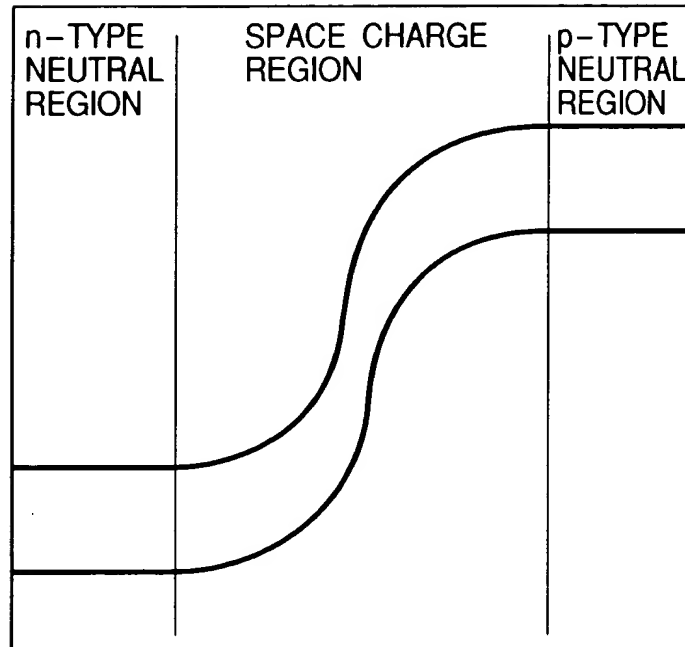
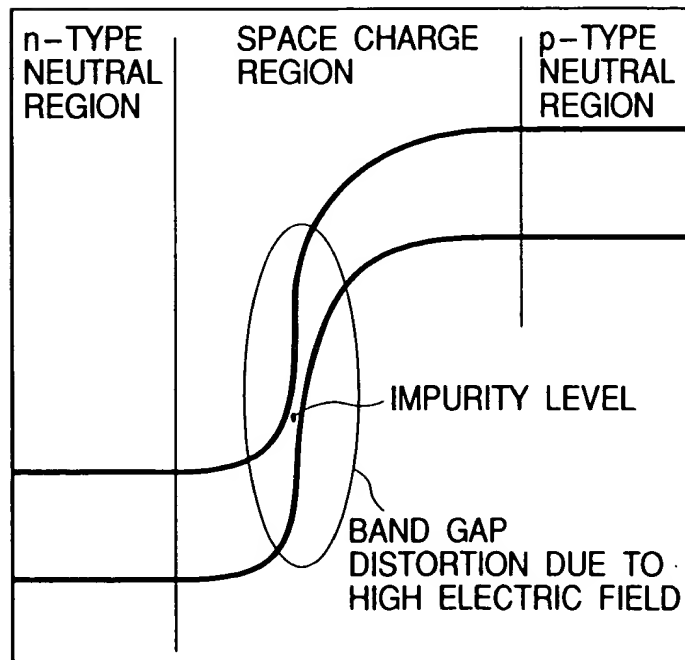
FIG. 33(a)*FIG. 33(b)*

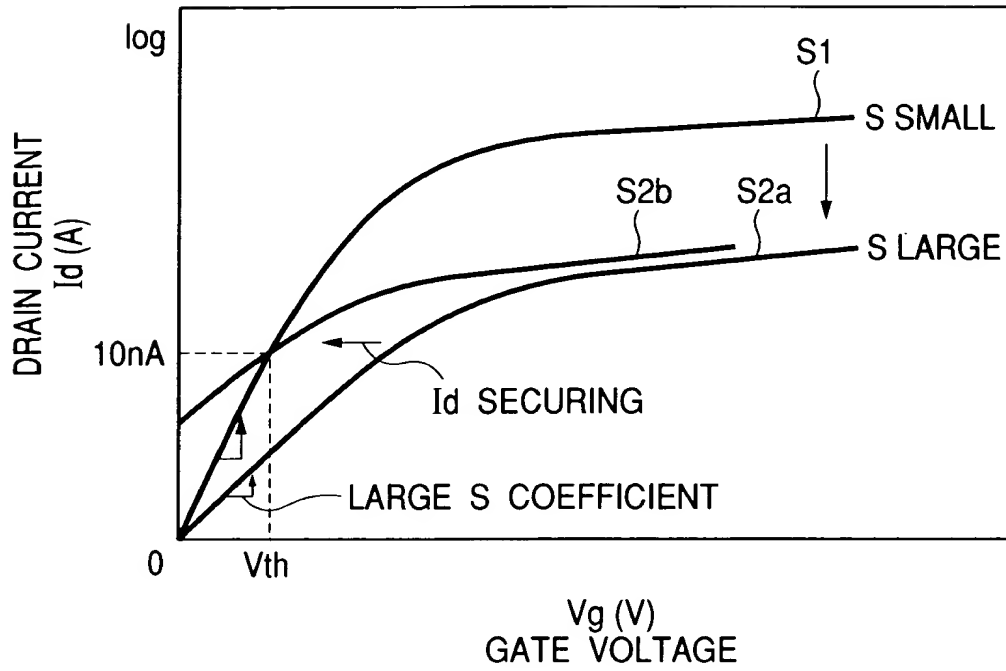
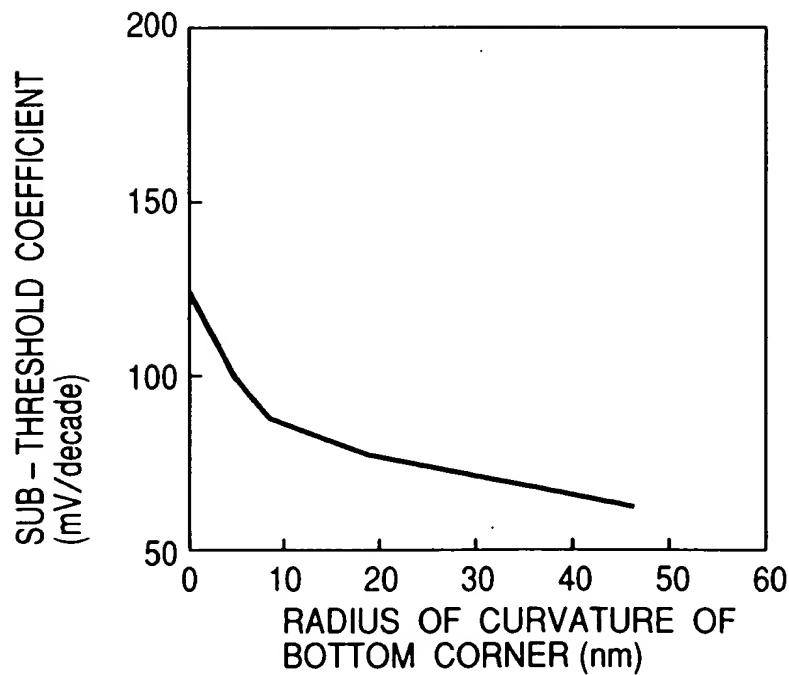
FIG. 34**FIG. 35**

FIG. 36

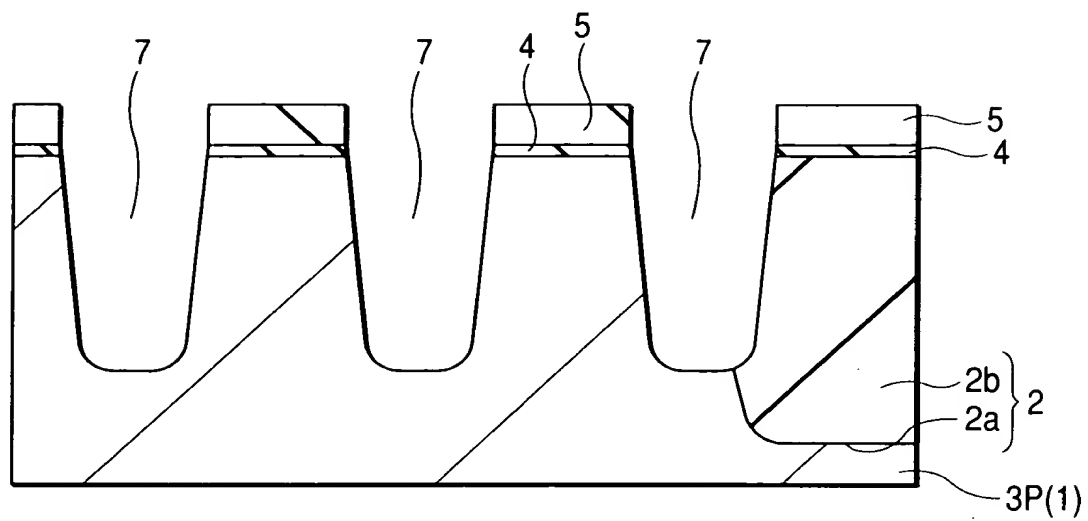


FIG. 37

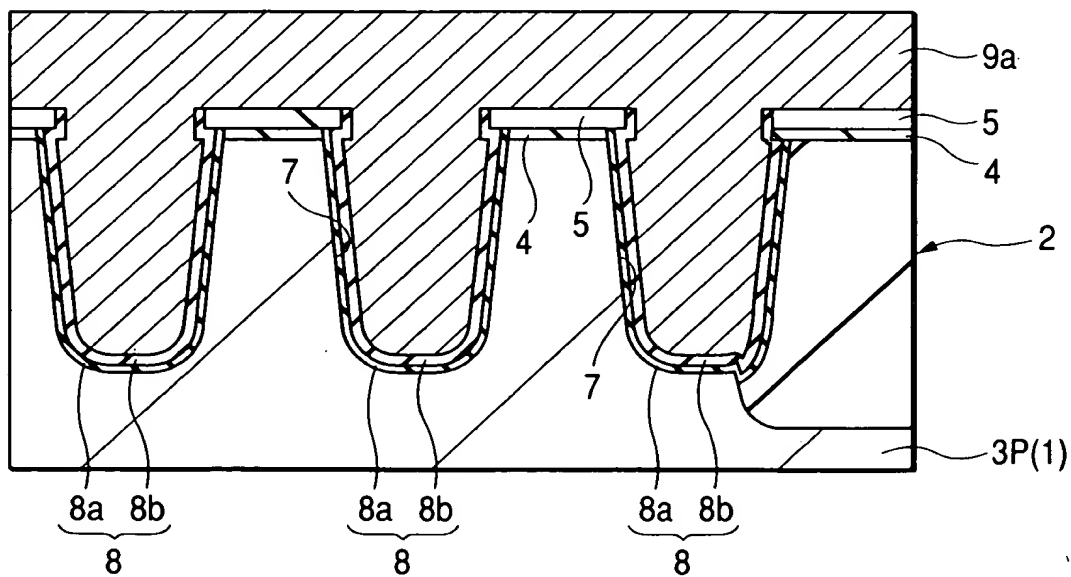


FIG. 38

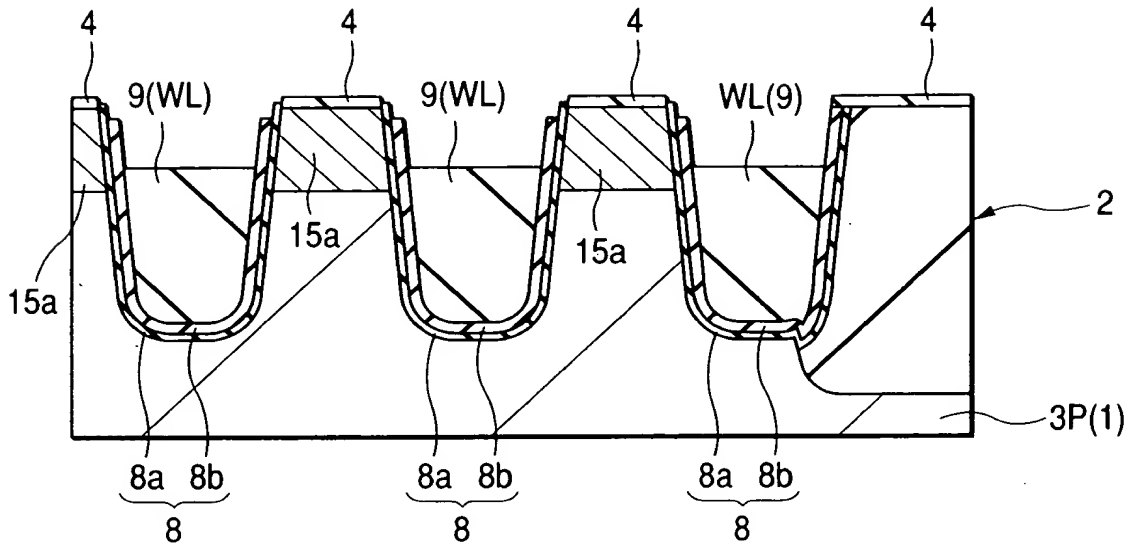


FIG. 39

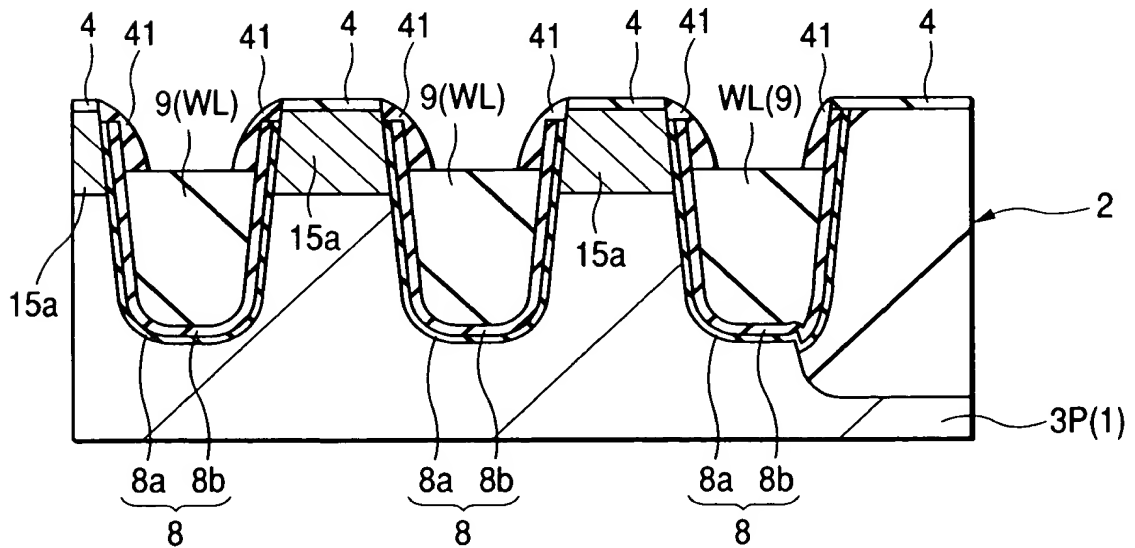


FIG. 40

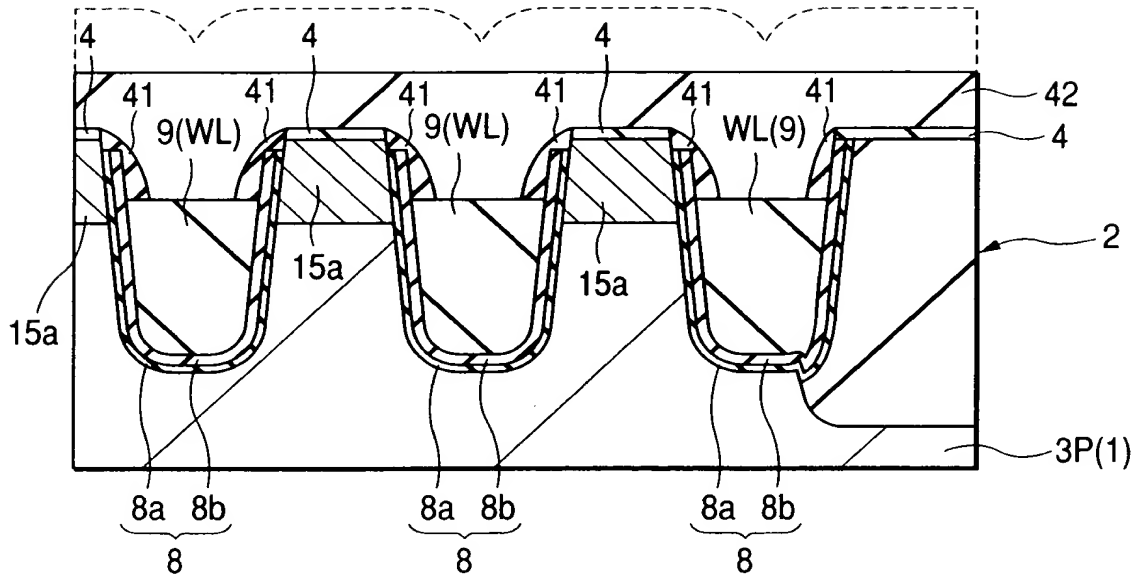


FIG. 41

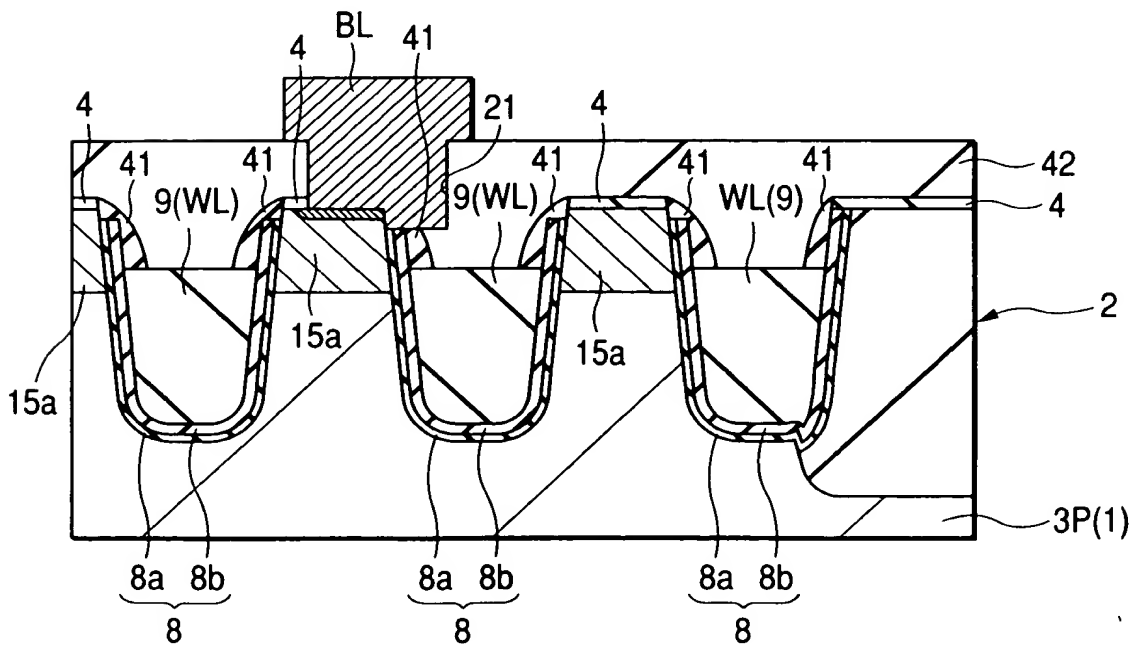


FIG. 42

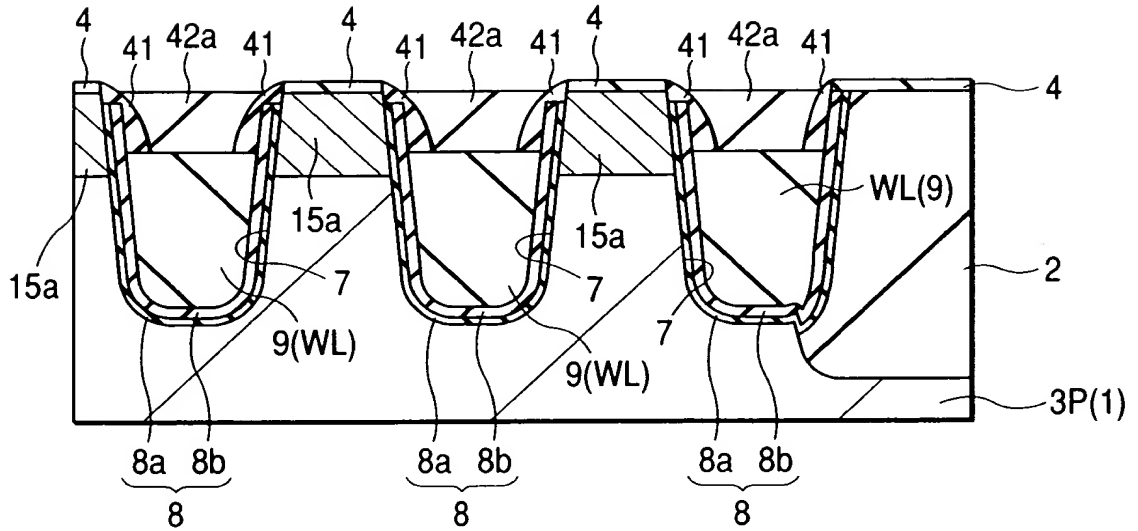


FIG. 43

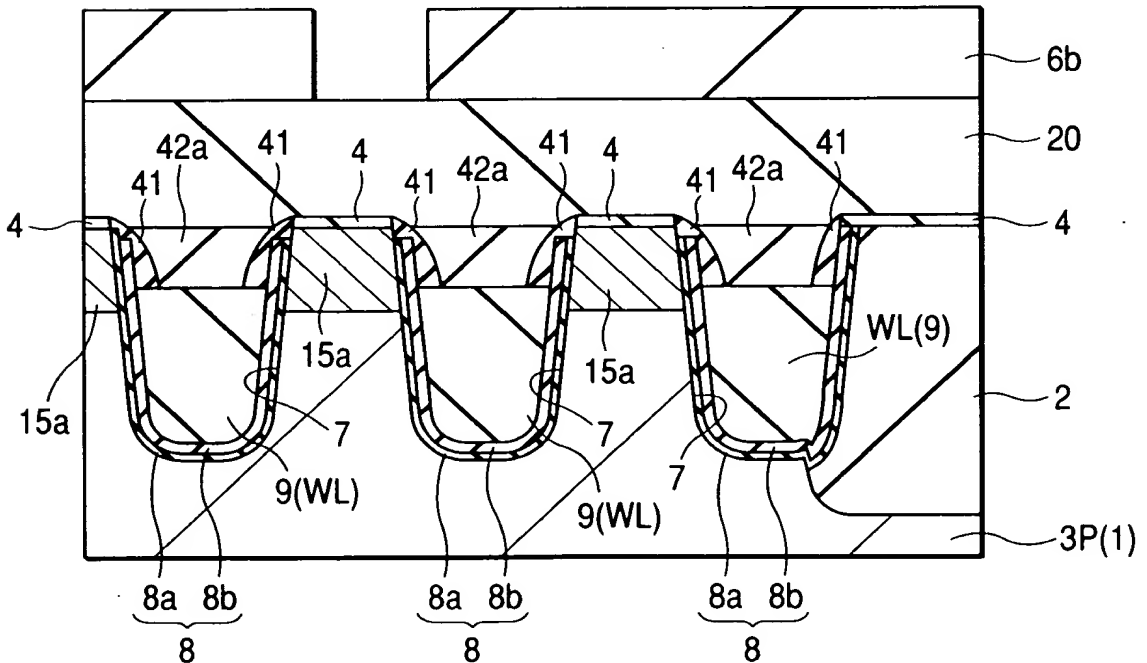


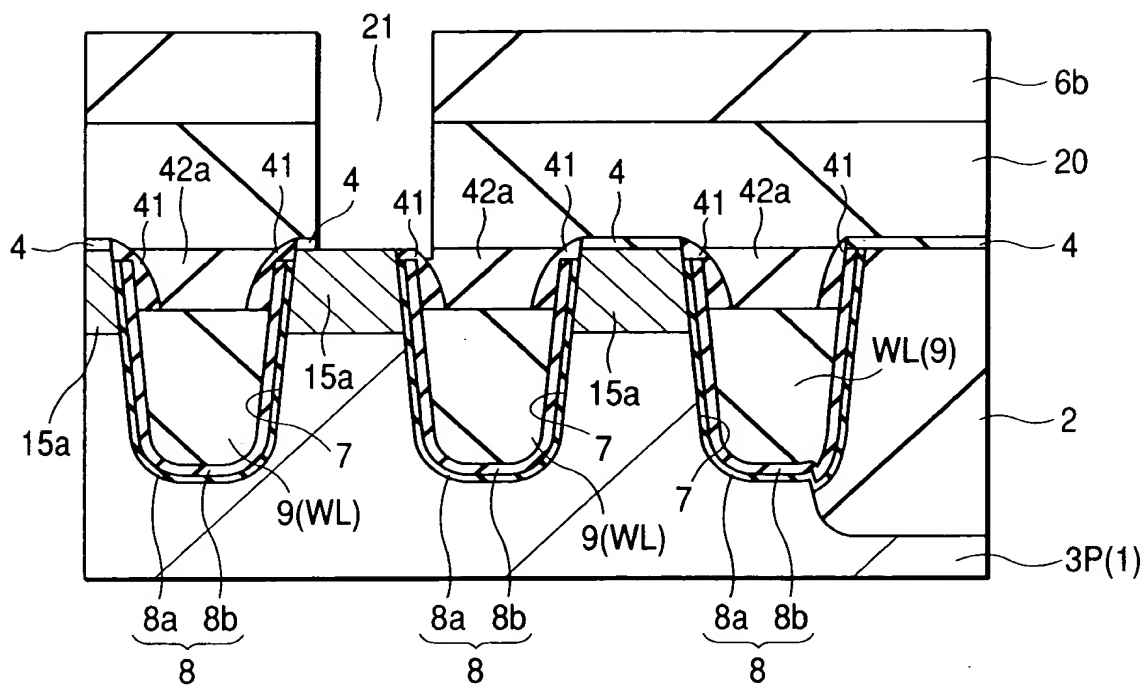
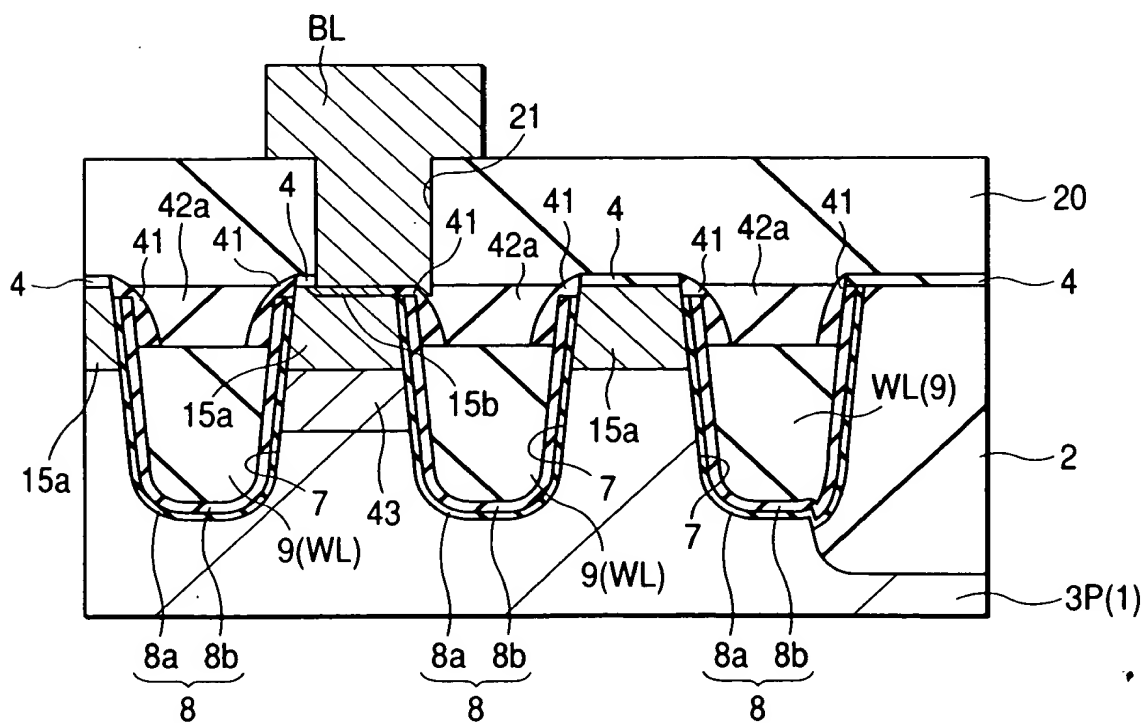
FIG. 44**FIG. 45**

FIG. 46

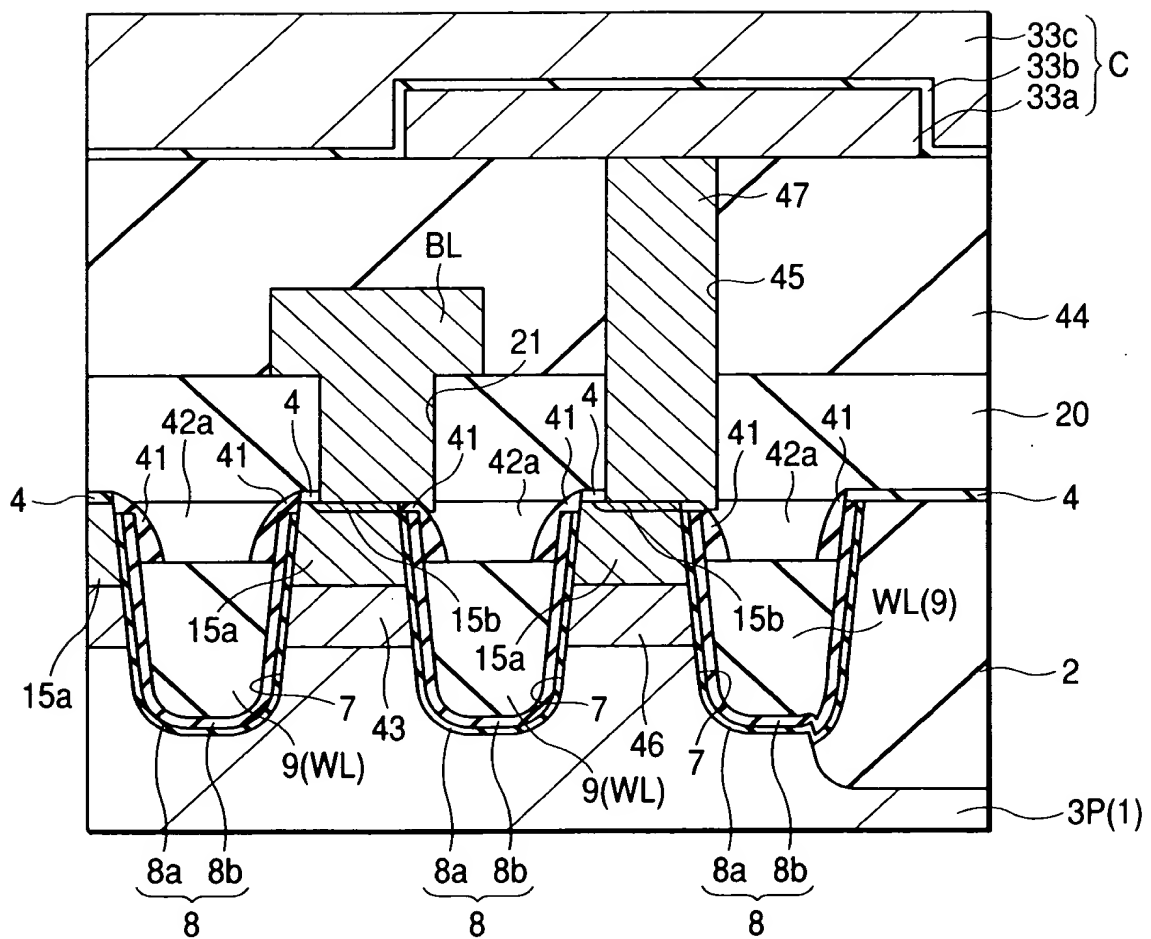


FIG. 48

